IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of)
) ATTN: APPLICATIONS BRANCH
YOSHIKAZU KUROSE)
)
Serial No. (Unassigned))
)
Filed: April 1, 1999)
)
For: IMAGE PROCESSING APPARATUS)
AND METHOD OF THE SAME)

LETTER TO THE OFFICIAL DRAFTSPERSON

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Approved
MP
7/29/01

Attached please find a copy of the proposed changes to the drawing(s) in this application, for which the approval of the Examiner is requested. Specifically, Figure 4 has been amended to show "Data Flip Flop (160 bit)".

Respectfully submitted,

DATE: April 1, 1999

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FIG. 1

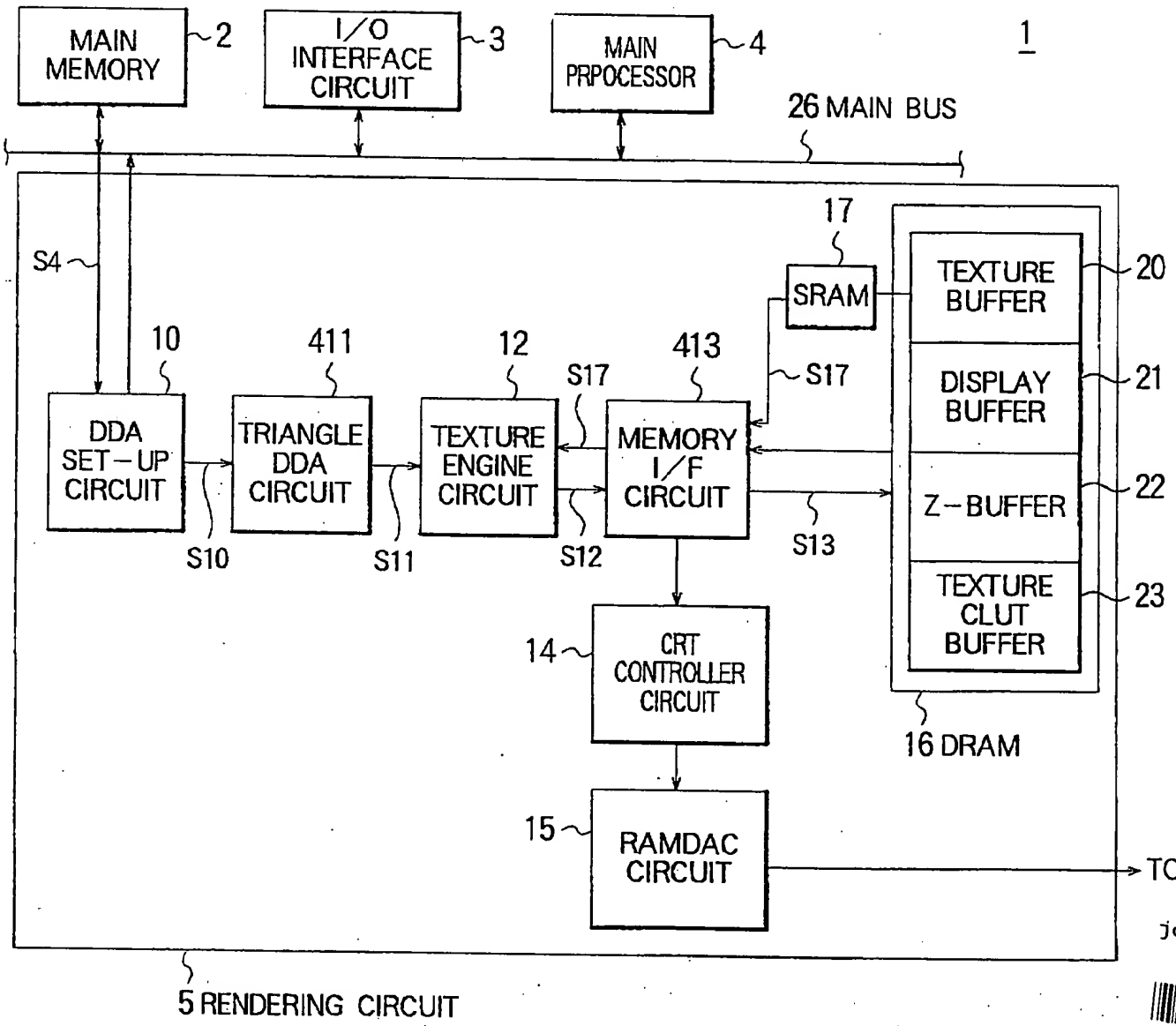

FIG. 2

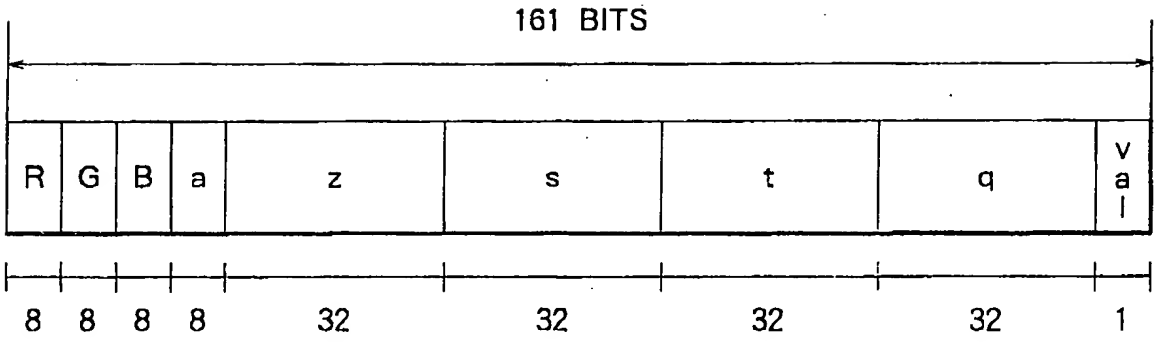

FIG. 3

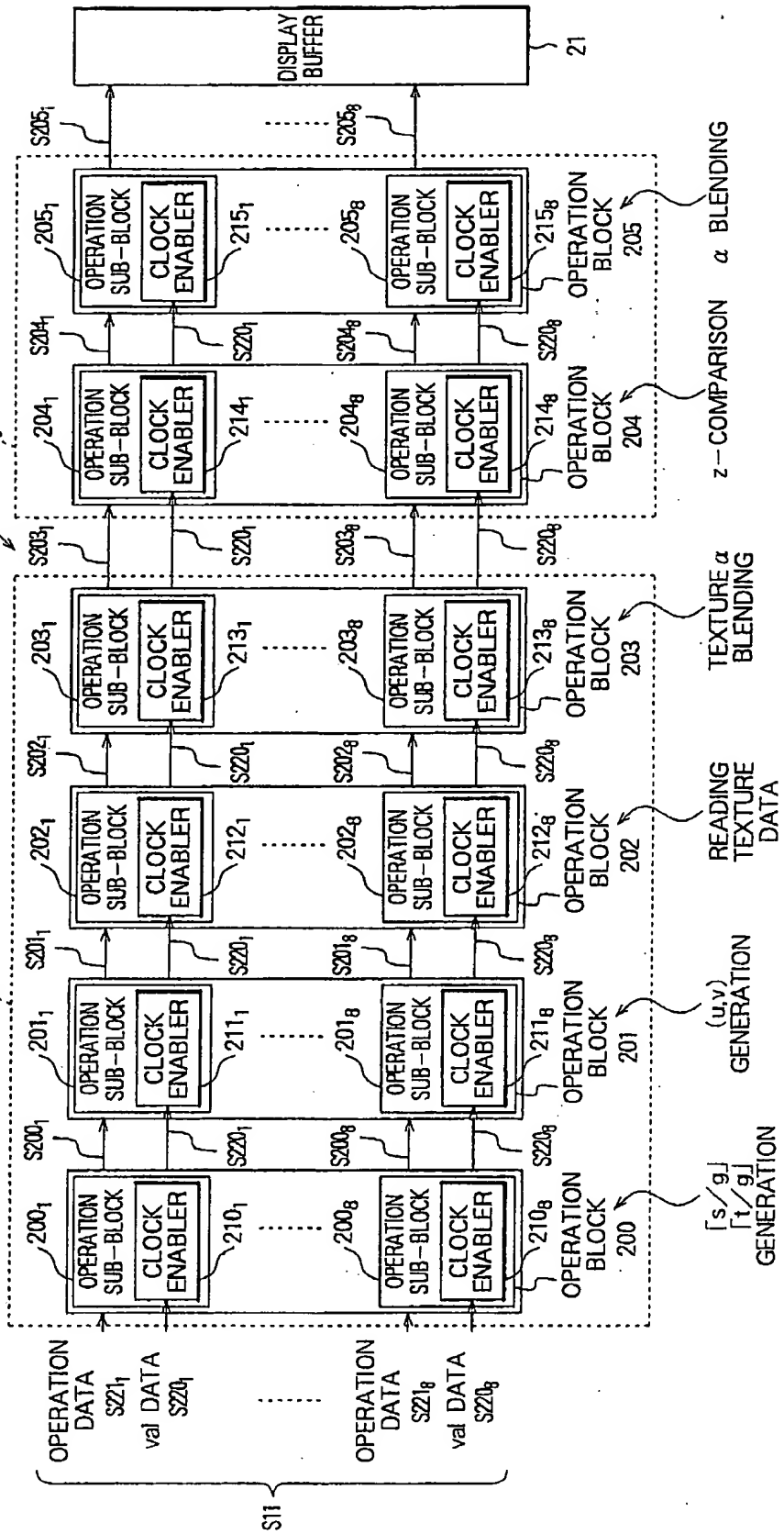
12 TEXTURE ENGINE CIRCUIT
13 MEMORY I/F CIRCUIT
S12
S11
OPERATION DATA
val DATA
OPERATION SUB-BLOCK
CLOCK ENABLER
OPERATION BLOCK
200
201
202
203
204
205
DISPLAY BUFFER
21
[s/g], [t/g] GENERATION
(u,v) GENERATION
READING TEXTURE DATA
TEXTURE α BLENDING
z-COMPARISON
α BLENDING

FIG. 4

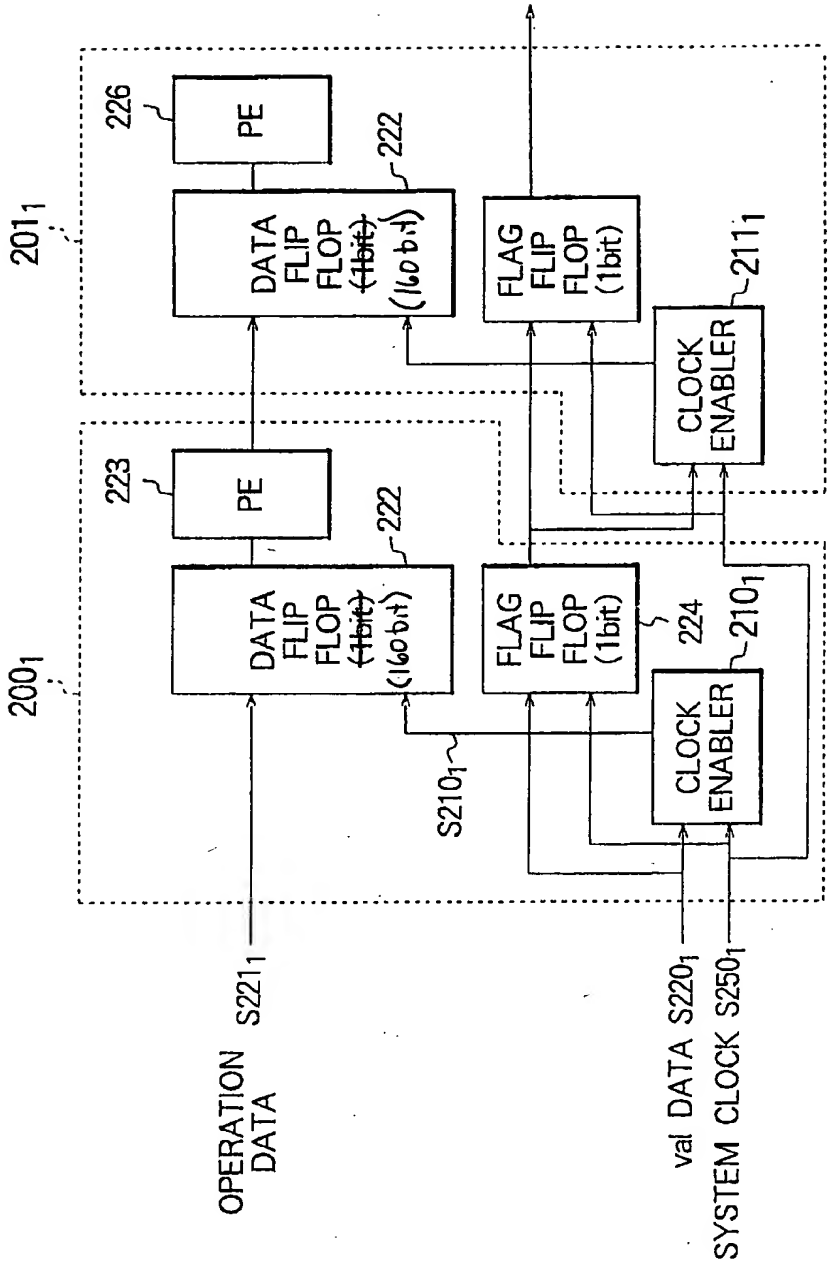
200_1
201_1
223
PE
222
DATA FLIP FLOP (1bit) (16bit)
226
PE
222
DATA FLIP FLOP (1bit) (16bit)
FLAG FLIP FLOP (1bit)
FLAG FLIP FLOP (1bit)
224
210_1
211_1
CLOCK ENABLER
CLOCK ENABLER
$S210_1$
OPERATION DATA $S221_1$
val DATA $S220_1$
SYSTEM CLOCK $S250_1$

FIG. 5

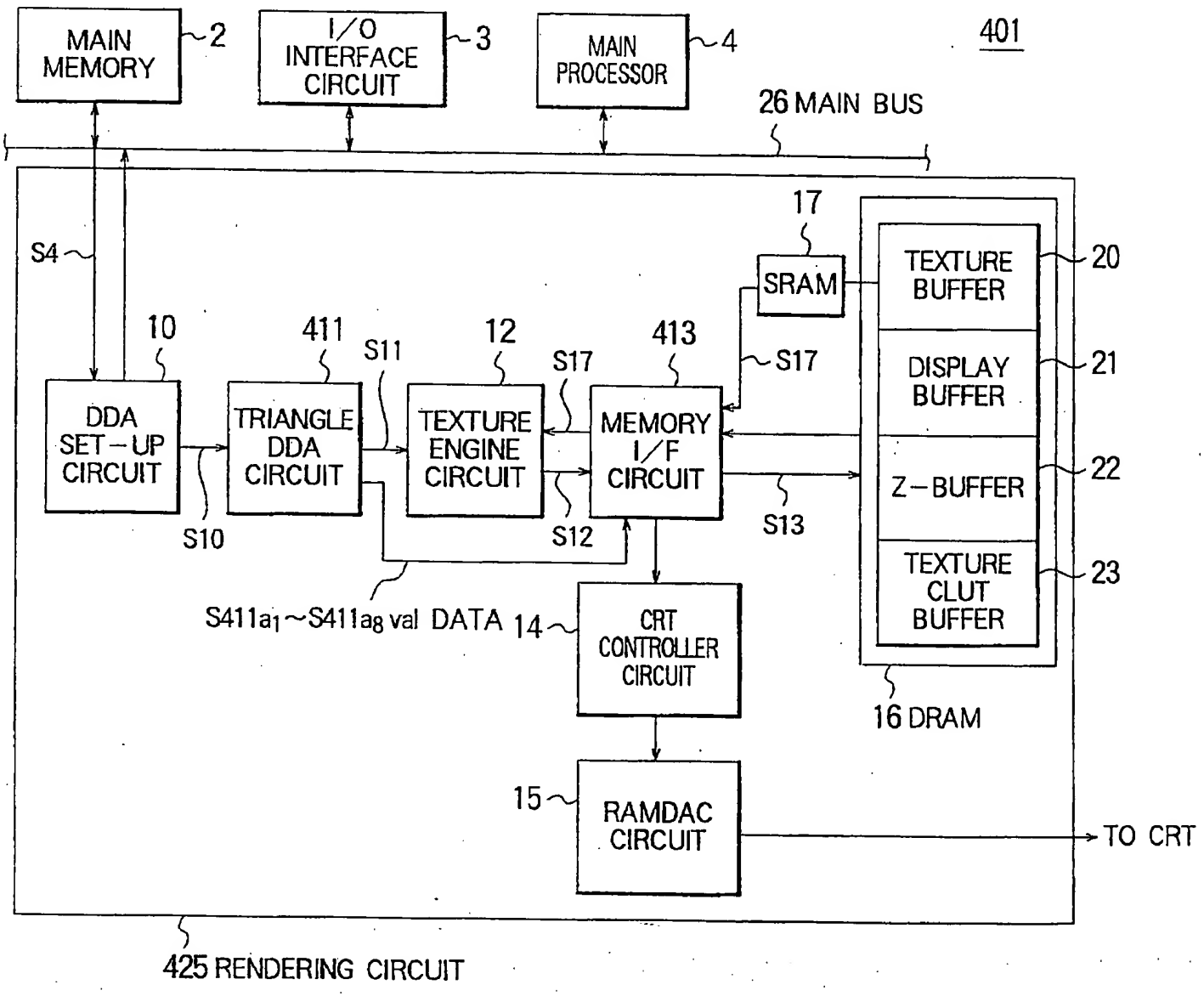
MAIN MEMORY
2
I/O INTERFACE CIRCUIT
3
MAIN PROCESSOR
4
401
26 MAIN BUS
17
SRAM
TEXTURE BUFFER
20
DISPLAY BUFFER
21
Z-BUFFER
22
TEXTURE CLUT BUFFER
23
16 DRAM
S4
10
411
S11
12
S17
413
S17
DDA SET-UP CIRCUIT
TRIANGLE DDA CIRCUIT
TEXTURE ENGINE CIRCUIT
MEMORY I/F CIRCUIT
S10
S12
S13
S411a1~S411a8 val DATA
14
CRT CONTROLLER CIRCUIT
15
RAMDAC CIRCUIT
TO CRT
425 RENDERING CIRCUIT

FIG. 6

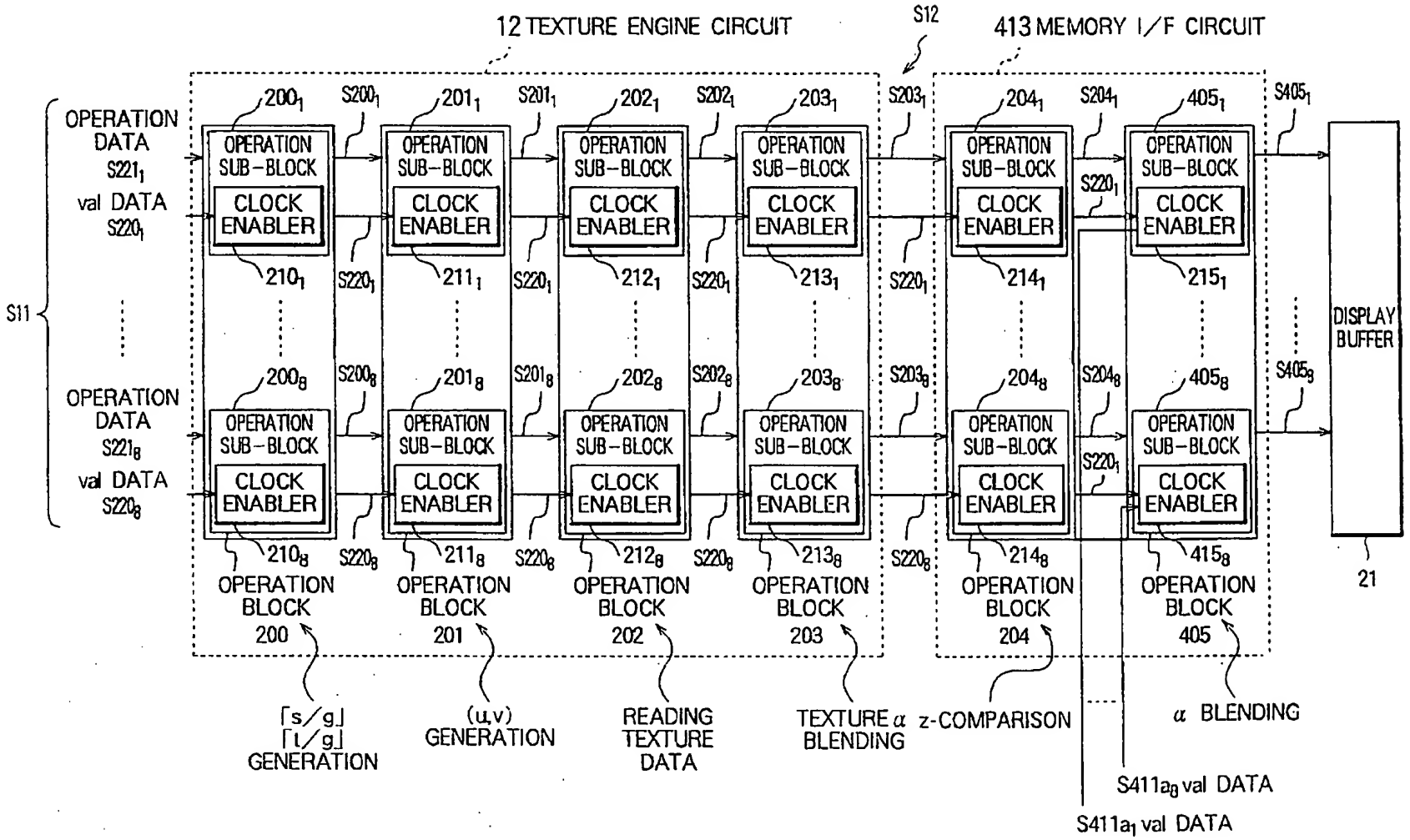
12 TEXTURE ENGINE CIRCUIT
S12
413 MEMORY I/F CIRCUIT
S11
OPERATION DATA S221₁
val DATA S220₁
OPERATION DATA S221₈
val DATA S220₈
OPERATION SUB-BLOCK
CLOCK ENABLER
200₁
201₁
202₁
203₁
204₁
405₁
210₁
211₁
212₁
213₁
214₁
215₁
200₈
201₈
202₈
203₈
204₈
405₈
210₈
211₈
212₈
213₈
214₈
415₈
S200₁
S201₁
S202₁
S203₁
S204₁
S405₁
S220₁
S200₈
S201₈
S202₈
S203₈
S204₈
S405₈
S220₈
DISPLAY BUFFER
21
OPERATION BLOCK 200
OPERATION BLOCK 201
OPERATION BLOCK 202
OPERATION BLOCK 203
OPERATION BLOCK 204
OPERATION BLOCK 405
⌈s/g⌋ ⌈t/g⌋ GENERATION
(u,v) GENERATION
READING TEXTURE DATA
TEXTURE α BLENDING
z-COMPARISON
α BLENDING
S411a₈ val DATA
S411a₁ val DATA

FIG. 7

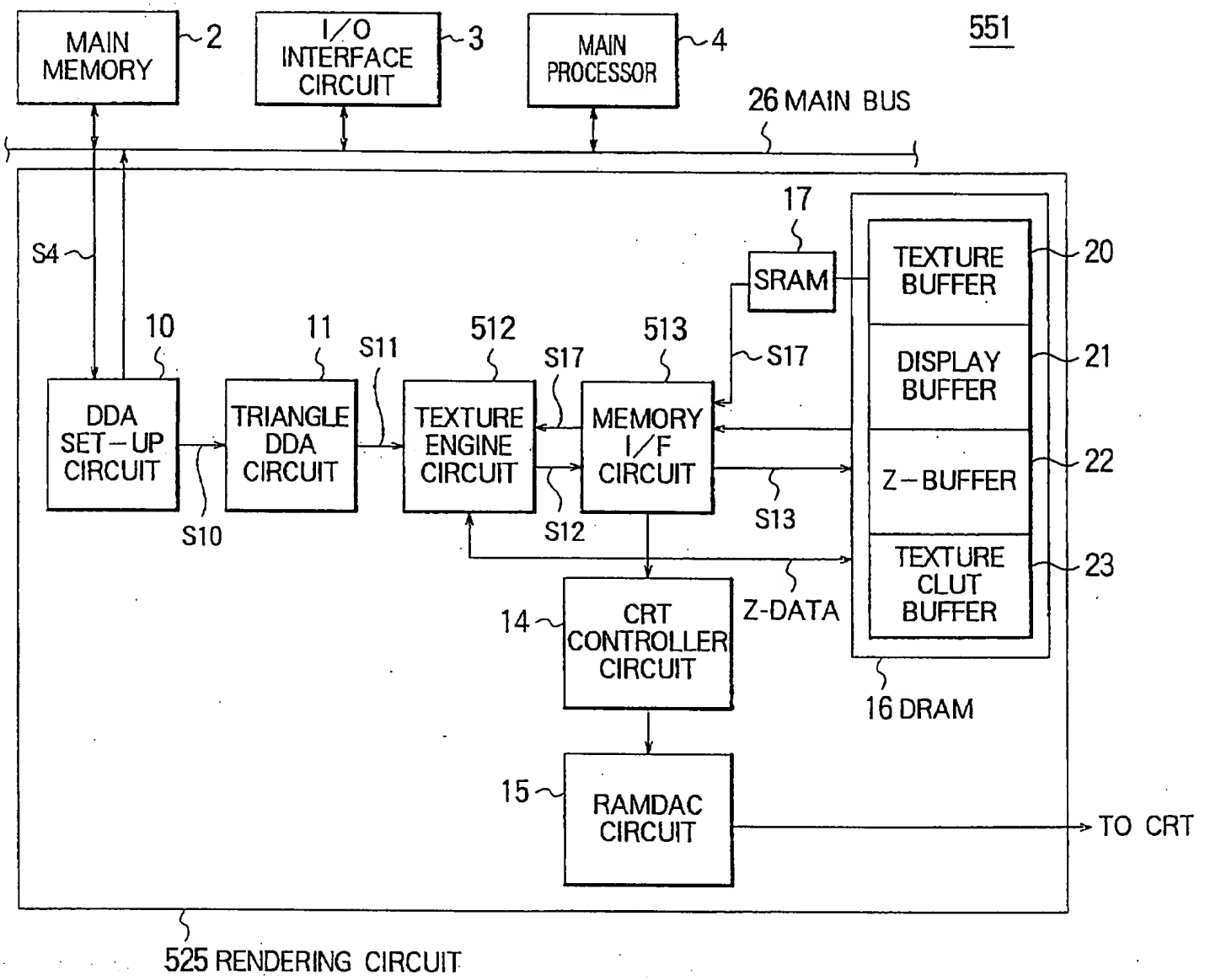
MAIN MEMORY
2
I/O INTERFACE CIRCUIT
3
MAIN PROCESSOR
4
551
26 MAIN BUS
17
SRAM
TEXTURE BUFFER
20
DISPLAY BUFFER
21
Z-BUFFER
22
TEXTURE CLUT BUFFER
23
16 DRAM
S4
10
DDA SET-UP CIRCUIT
S10
11
TRIANGLE DDA CIRCUIT
S11
512
TEXTURE ENGINE CIRCUIT
S12
S17
513
MEMORY I/F CIRCUIT
S13
S17
Z-DATA
14
CRT CONTROLLER CIRCUIT
15
RAMDAC CIRCUIT
TO CRT
525 RENDERING CIRCUIT

FIG. 8

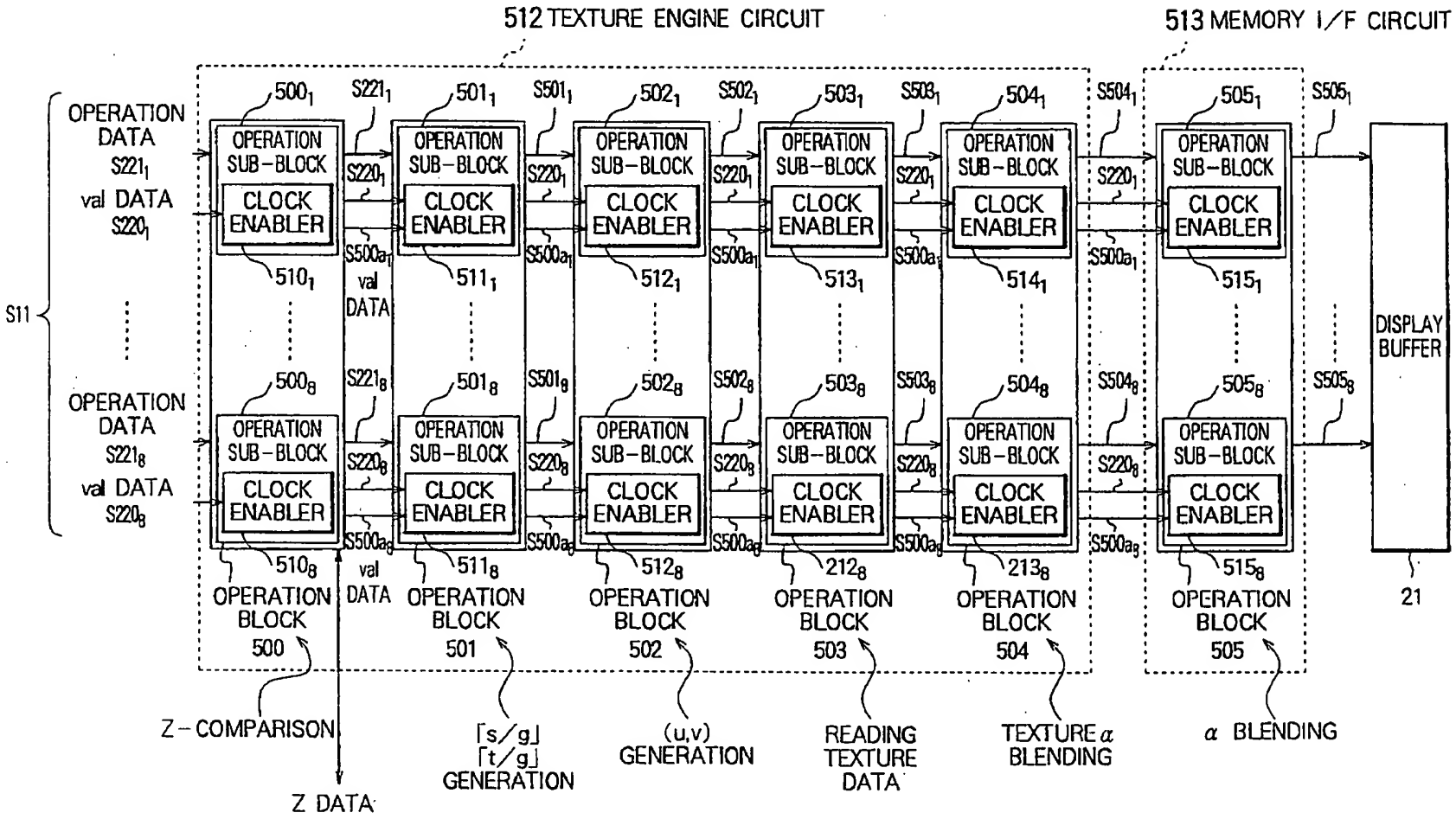
512 TEXTURE ENGINE CIRCUIT
513 MEMORY I/F CIRCUIT
OPERATION DATA S221₁
val DATA S220₁
OPERATION DATA S221₈
val DATA S220₈
S11
OPERATION SUB-BLOCK
CLOCK ENABLER
DISPLAY BUFFER
21
OPERATION BLOCK 500
OPERATION BLOCK 501
OPERATION BLOCK 502
OPERATION BLOCK 503
OPERATION BLOCK 504
OPERATION BLOCK 505
val DATA
Z DATA
Z-COMPARISON
⌈s/g⌋ ⌈t/g⌋ GENERATION
(u,v) GENERATION
READING TEXTURE DATA
TEXTURE α BLENDING
α BLENDING

FIG. 9

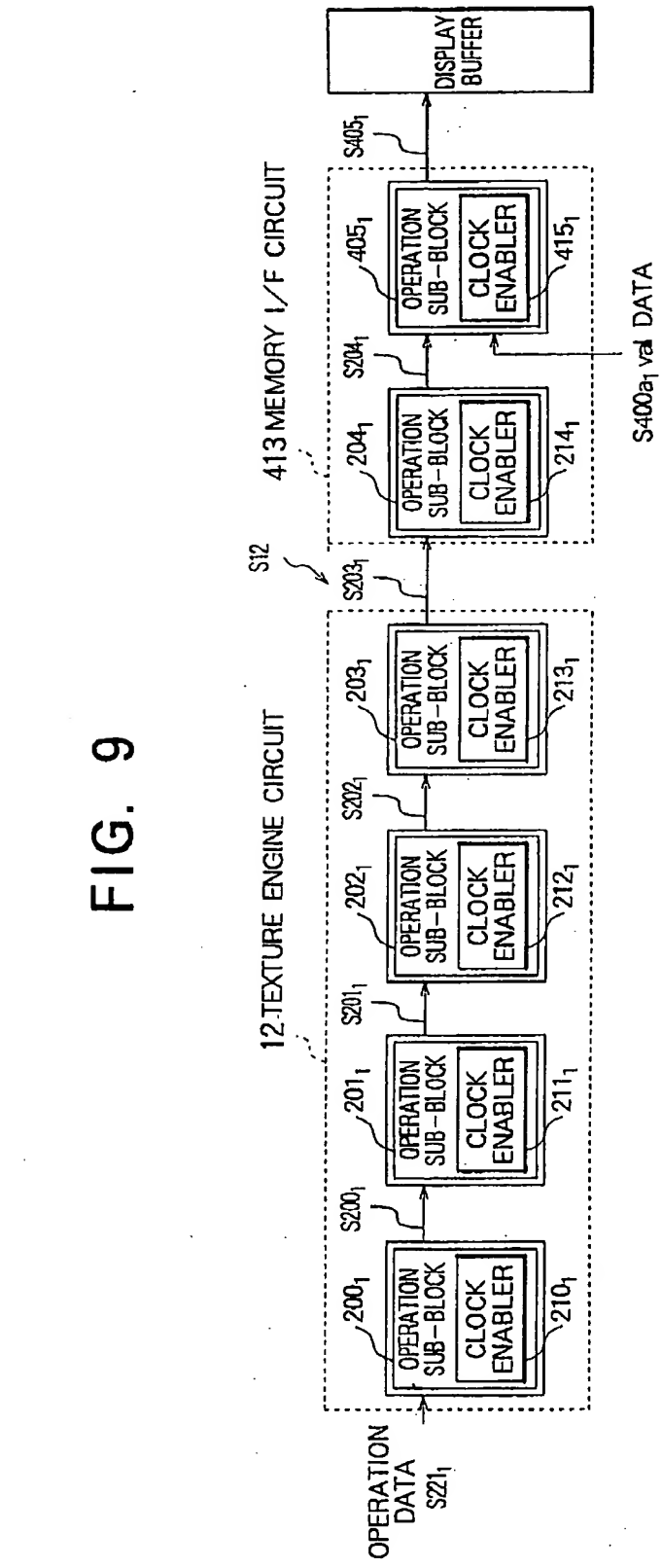
DISPLAY BUFFER
413 MEMORY I/F CIRCUIT
12 TEXTURE ENGINE CIRCUIT
S12
OPERATION DATA S221
OPERATION SUB-BLOCK
CLOCK ENABLER
S400a1 val DATA

FIG. 10

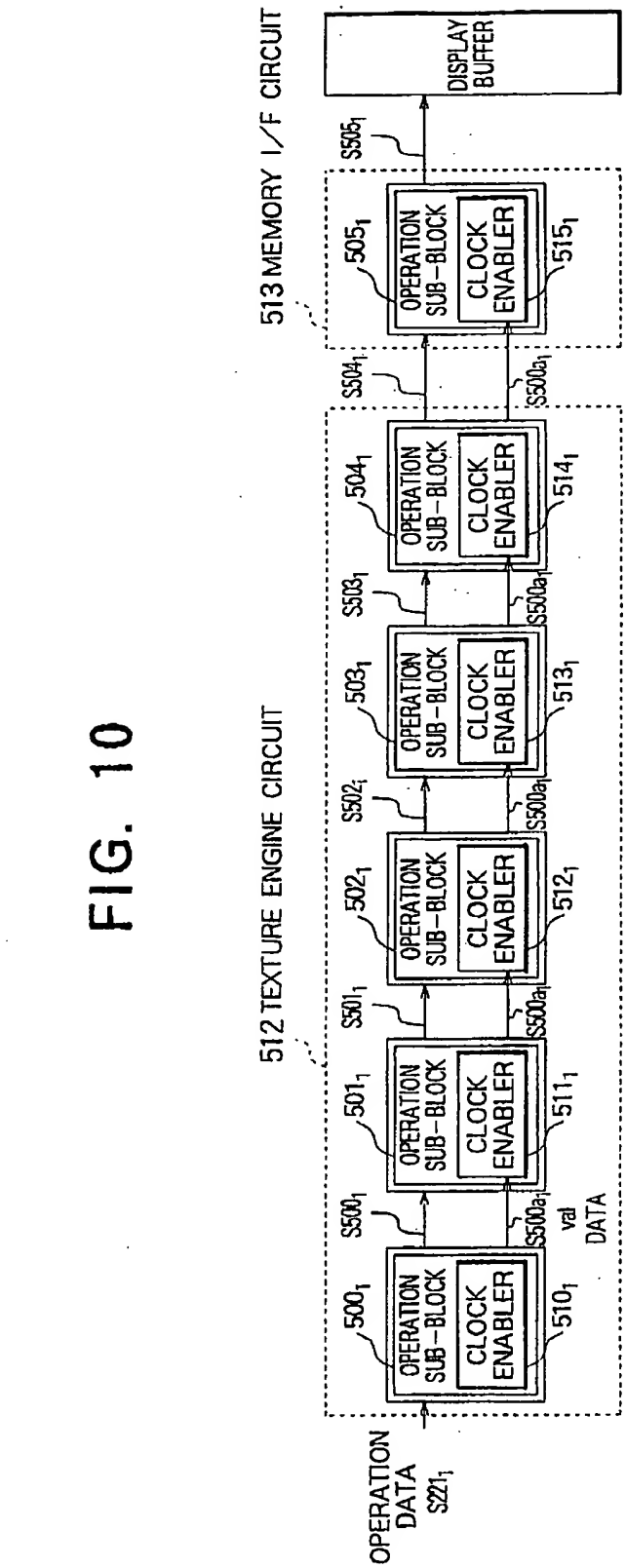
512 TEXTURE ENGINE CIRCUIT
513 MEMORY I/F CIRCUIT
OPERATION DATA S221₁
OPERATION SUB-BLOCK
CLOCK ENABLER
500₁
510₁
S500₁
501₁
511₁
S501₁
502₁
512₁
S502₁
503₁
513₁
S503₁
504₁
514₁
S504₁
505₁
515₁
S505₁
S500a₁
val
DATA
DISPLAY BUFFER

FIG. 11

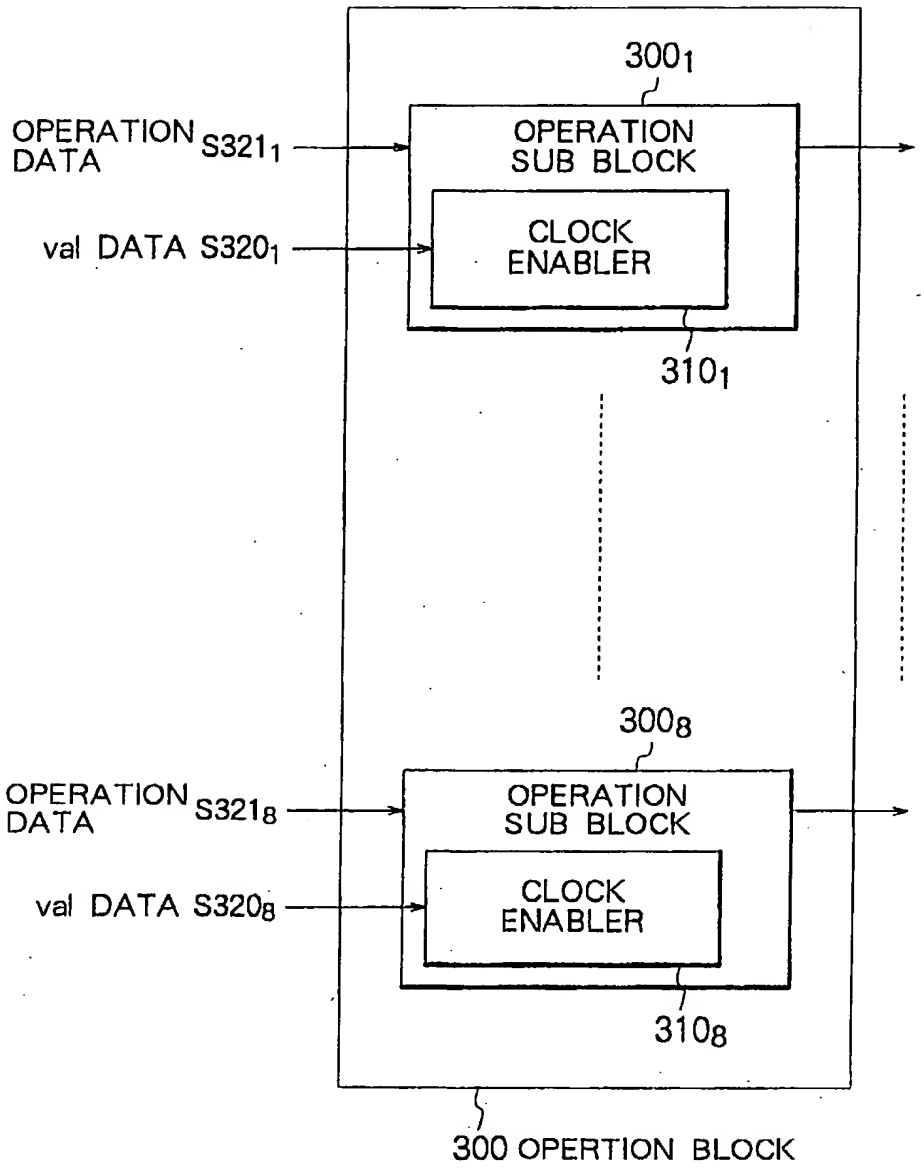
300_1
OPERATION DATA $S321_1$
OPERATION SUB BLOCK
val DATA $S320_1$
CLOCK ENABLER
310_1
300_8
OPERATION DATA $S321_8$
OPERATION SUB BLOCK
val DATA $S320_8$
CLOCK ENABLER
310_8
300 OPERTION BLOCK

FIG. 12